Famiglie logiche:

Inizio '900: Rele'
(es. centralini telefonici, Z3 (Germania - 1941))

Anni '40-'50: Tubi a vuoto
(es. ENIAC (US - 1946))

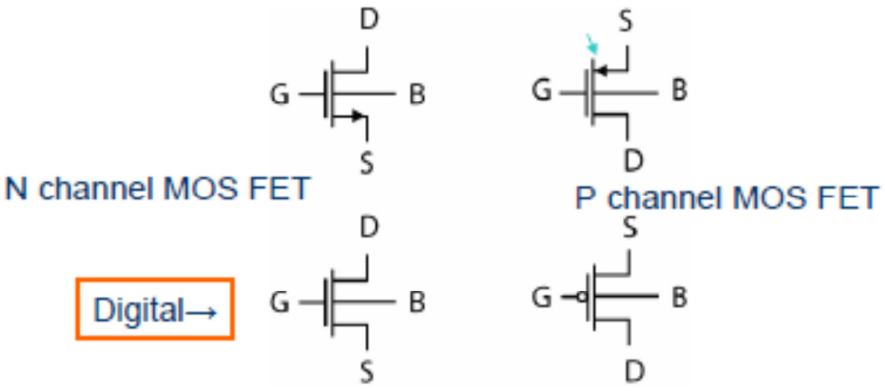
Anni '60: Transistor
(Discreti, poi integrati - Es. RTL, DTL, TTL,...)

Anni '70 - '80: PMOS, NMOS
(Zilog Z80, Intel 8080, Motorola 6502, Fairchild F8, ..)

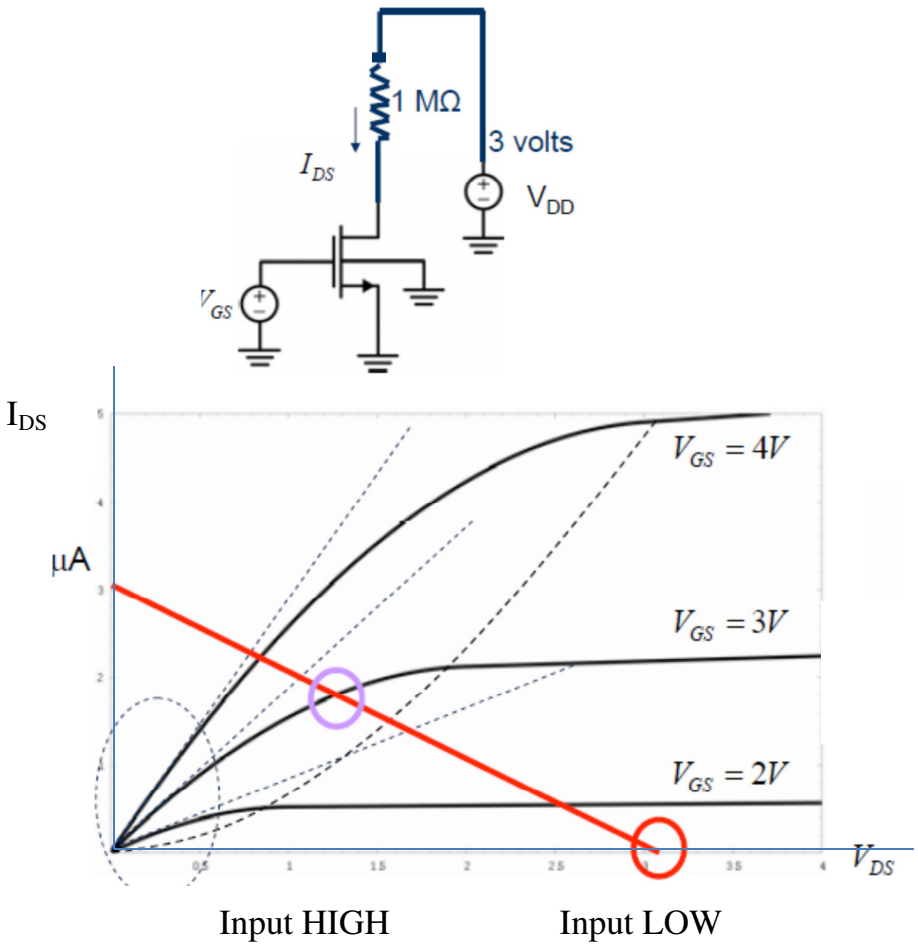
Anni '90 $\rightarrow$: CMOS
$\sim$ Tutto!

MOS usati come interruttori:

NMOS ON per VG +va
PMOS ON per VG -va
Simboli in applicazioni digitali:



Inverter NMOS:



Input HIGH Input LOW

→ Per input *HIGH*, output *LOW* ~ 1.2 *V* → Non esattamente 0 *V*

→ Stadio successivo pilotato da un *LOW* troppo alto

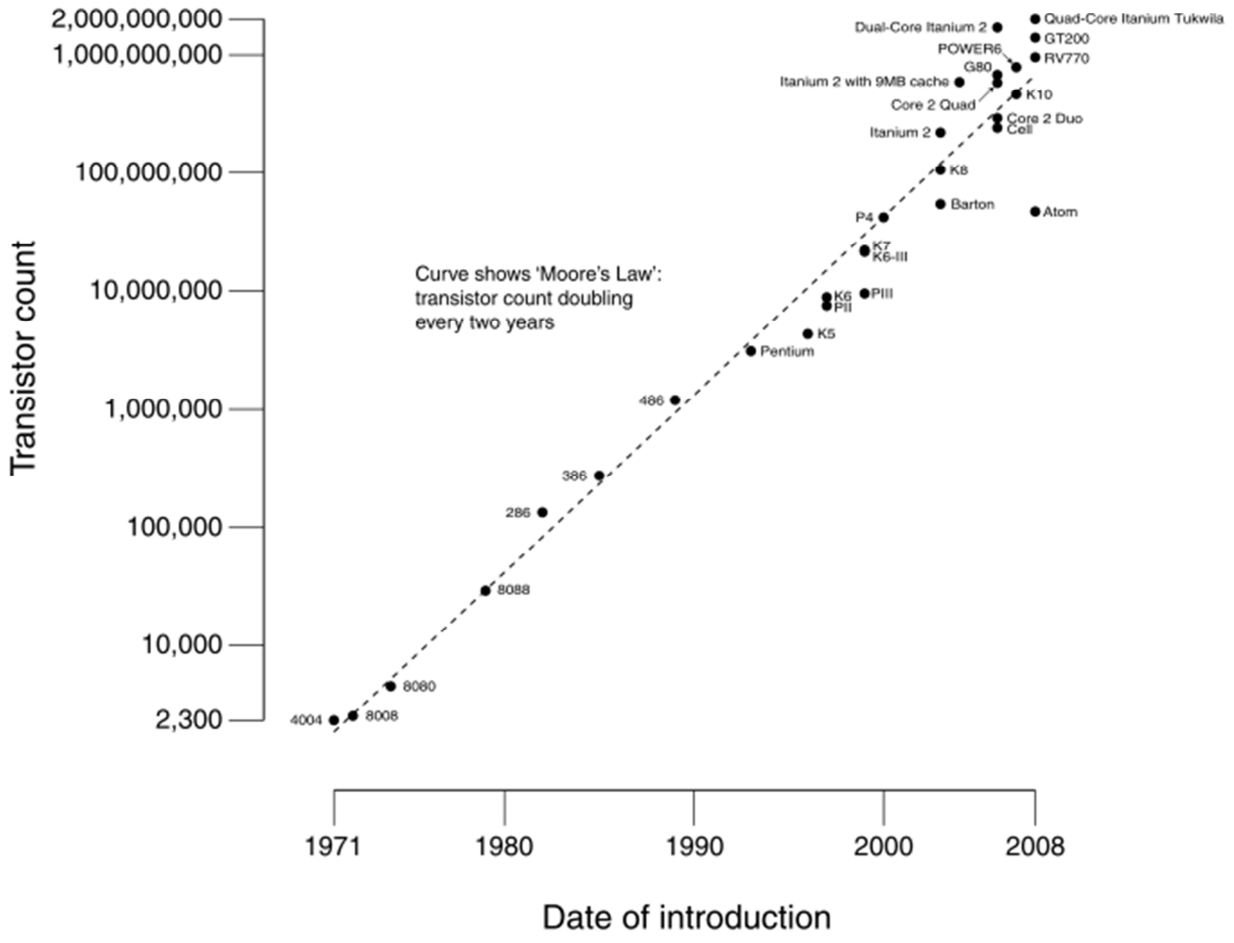
Inoltre:

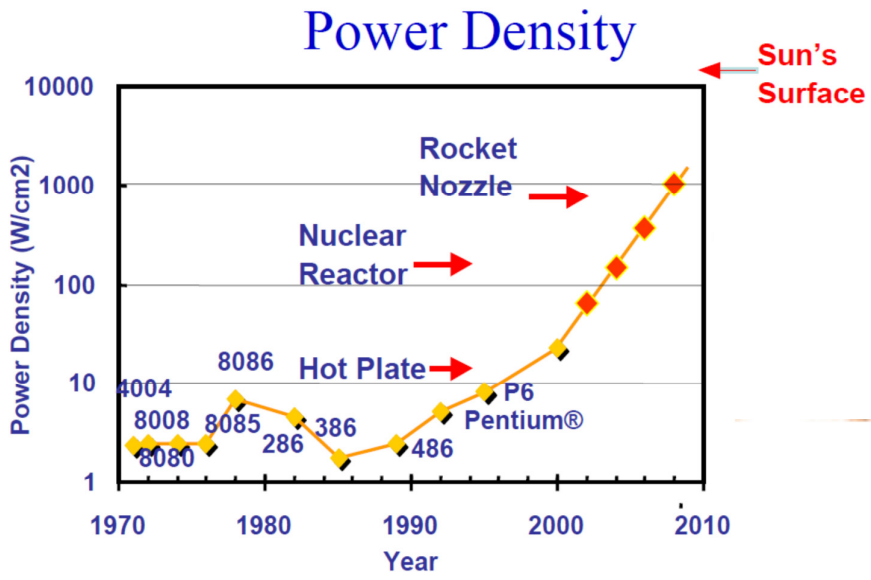
R grandi: difficili e non benvenute

$I_{LOW} \sim 3\mu A \rightarrow P_{inv} \sim 10\mu W \rightarrow P_{tot} \sim 1\ W / 10^5 transistor$

[1 *CPU* di oggi ~ 10 *kW !*]

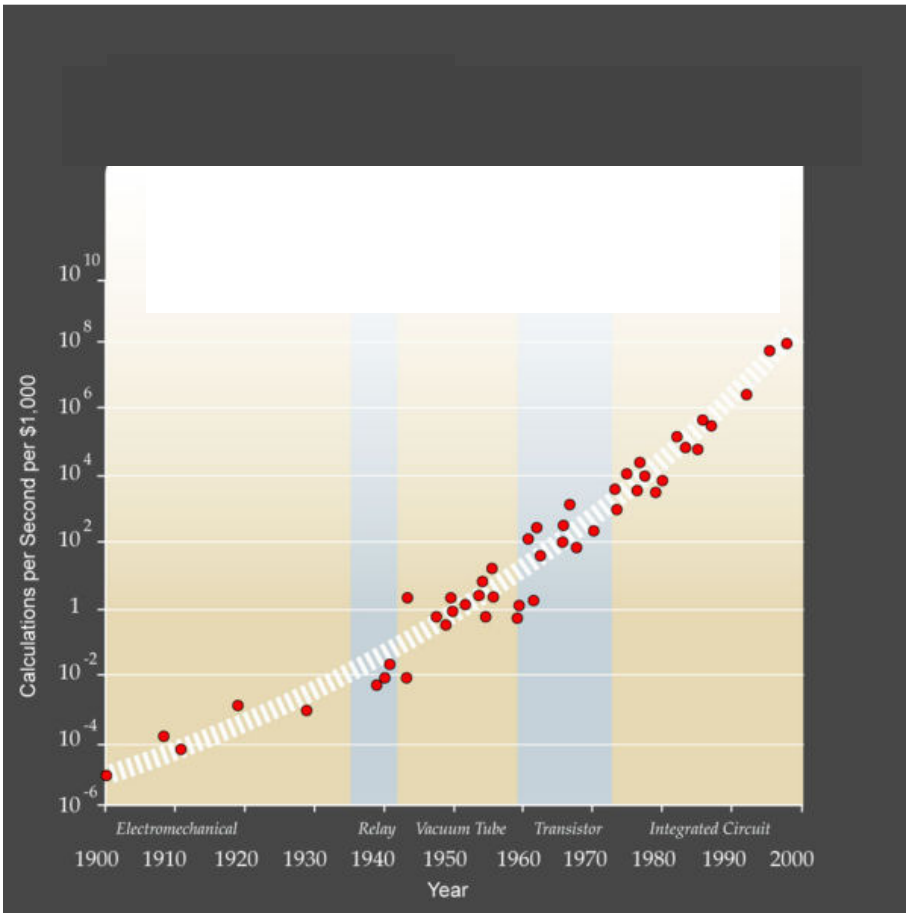
CPU Transistor Counts 1971-2008 & Moore's Law



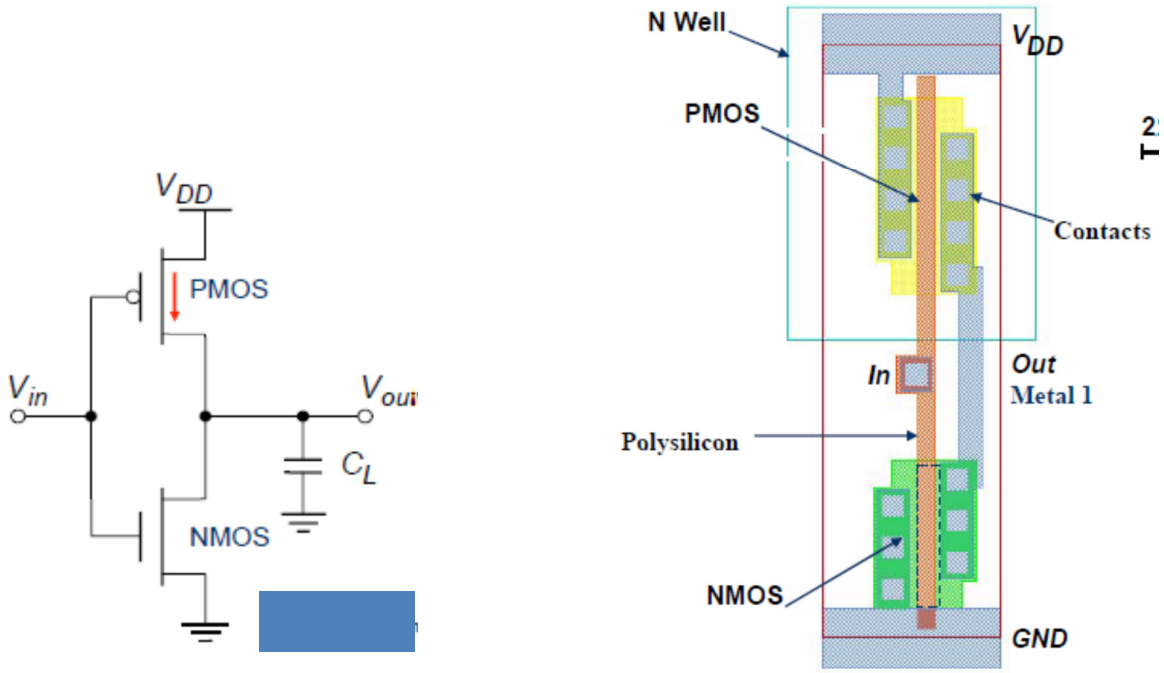


Effetto della crescente integrazione:

Un secolo di incremento esponenziale nella velocita' di calcolo



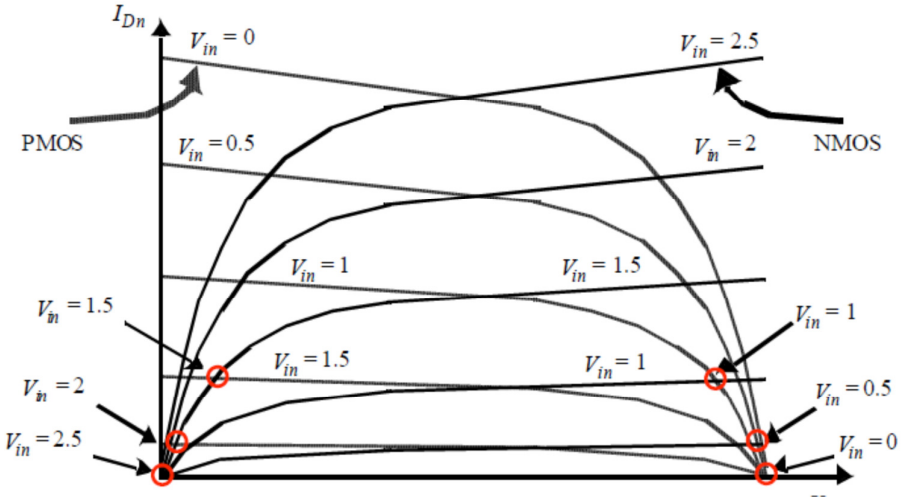
Inverter CMOS:



Ognuno dei 2 MOS: carico dell'altro

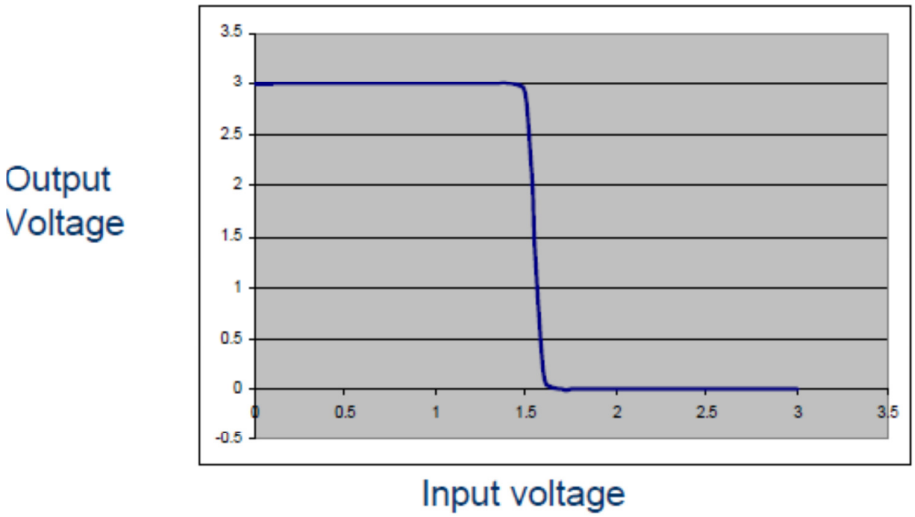
Fissata $V_{in} = \begin{cases} V_{GS}^N \\ V_{DD} - V_{GS}^P \end{cases}$

→ Intersezione delle caratteristiche = Stato dei 2 MOS

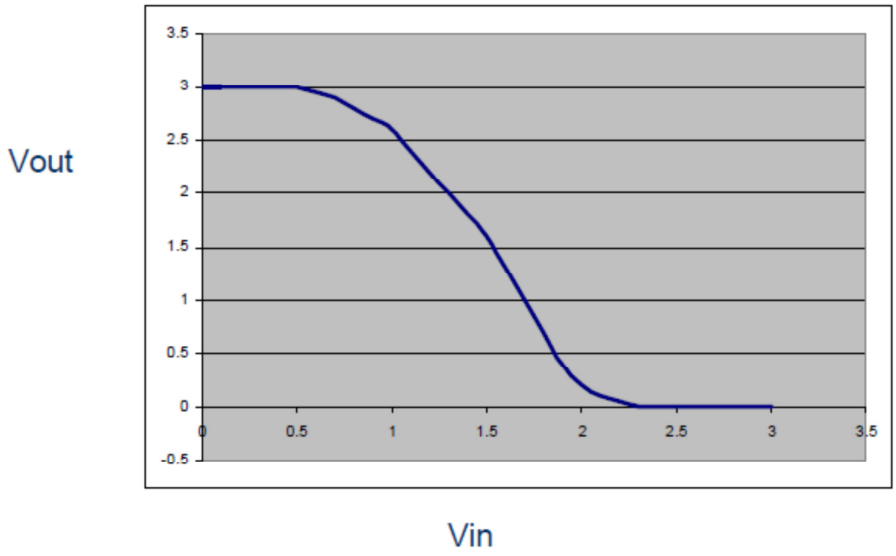


→ Con livelli logici $\begin{cases} HIGH = 2.5\ V \\ LOW = 0\ V \end{cases} : \begin{matrix} V_{in} = HIGH \rightarrow V_{out} = LOW \\ V_{in} = LOW \rightarrow V_{out} = HIGH \end{matrix} \rightarrow OK$

Risposta in/out di un inverter 'ideale':



Risposta in/out di un inverter CMOS:



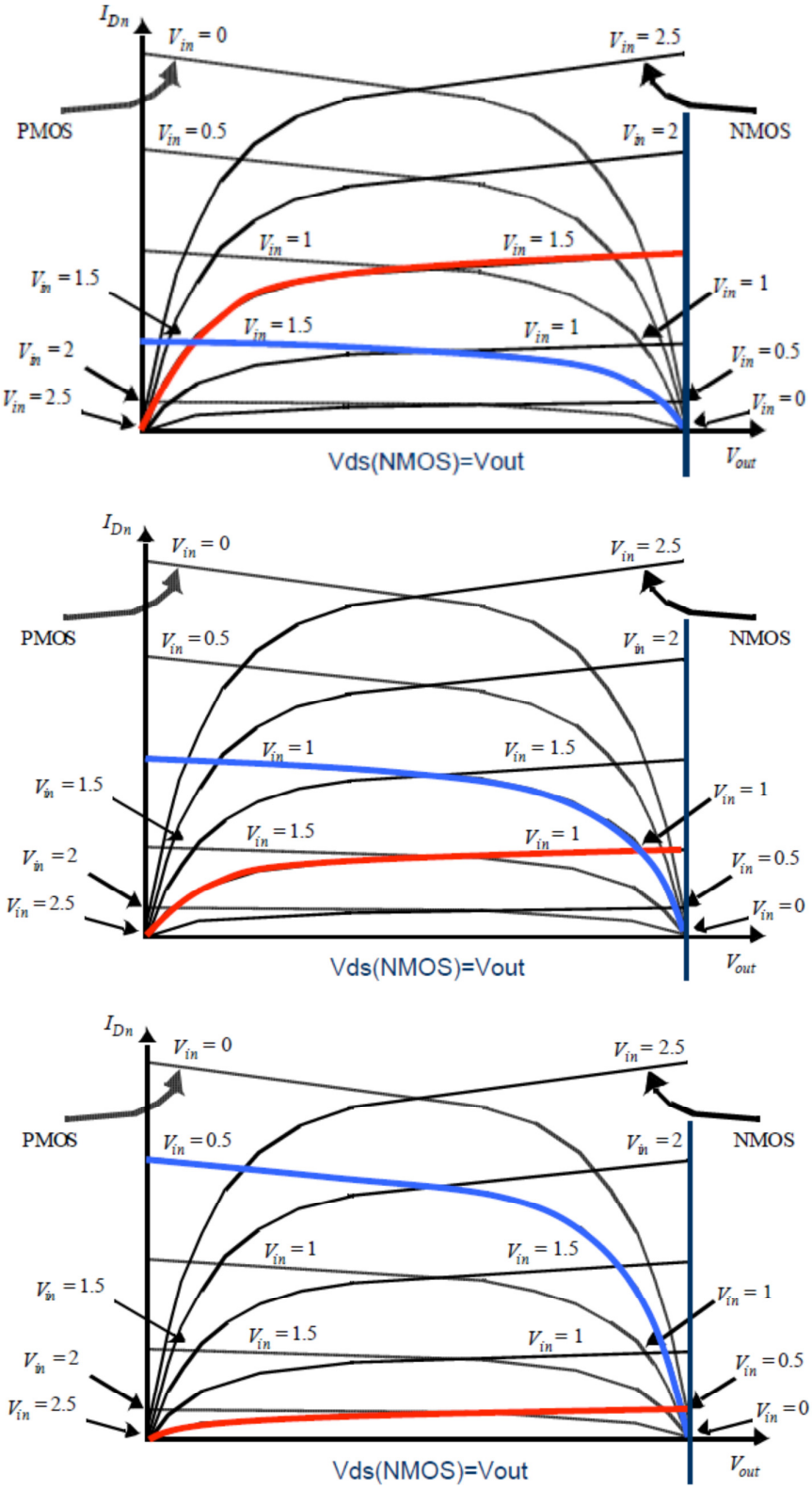
→ Non ideale, accettabile

Interdizione di N/P con V_{in} *LOW* / *HIGH*

→ $I = 0$ tranne durante le transizioni

→ No dissipazione statica (solo minimo effetto dovuto alle correnti di leakage)

Stato dell'inverter per valori intermedi di V_{in}:



Dissipazione dinamica:

Correnti durante transizione $LOW \leftrightarrow HIGH$:

Carica/Scarica della capacita' di uscita

$$C_L = C_{out}^{inv} + \underbrace{C_{in}^{inv}}_{\text{stadio seguente}}$$

Potenza istantanea dissipata nel PMOS durante transizione $LOW \rightarrow HIGH$:

$$P_P = i_L \left(V_{DD} - V_{out}\right)$$

$$i_L = C_L \frac{dV_{out}}{dt}$$

$$\rightarrow P_P = C_L \frac{dV_{out}}{dt}\left(V_{DD} - V_{out}\right)$$

Energia dissipata nel PMOS:

$$\rightarrow E_P = \int_0^{\infty} P_P dt = \int_0^{\infty} C_L \frac{dV_{out}}{dt}\left(V_{DD} - V_{out}\right)dt = \int_0^{V_{DD}} C_L \left(V_{DD} - V_{out}\right)dV_{out}$$

$$\rightarrow E_P = C_L V_{DD}^2 - \frac{1}{2} C_L V_{DD}^2 = \frac{1}{2} C_L V_{DD}^2$$

Energia dissipata nel NMOS:

$$E_N = \frac{1}{2} C_L V_{DD}^2$$

$\rightarrow$ Energia dissipata nell'inverter:

$E = E_P + E_N = C_L V_{DD}^2$ per transizione

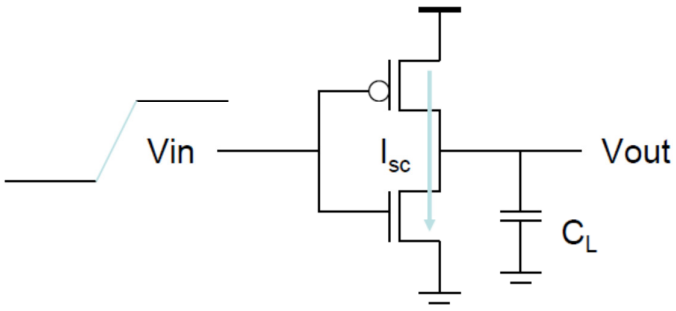
Con f transizioni al secondo:

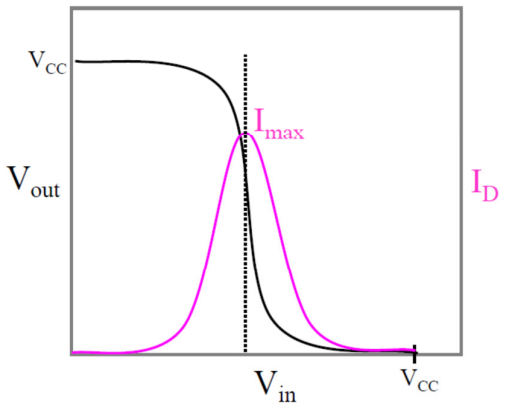
$P = f C_L V_{DD}^2$ potenza dissipata

Dissipazione *Short - Circuit*:
Dovuta a durata finita delle transizioni

Stati intermedi dell'inverter: NMOS + PMOS in conduzione

Effetto tanto piu' grande quanto piu' lente le transizioni

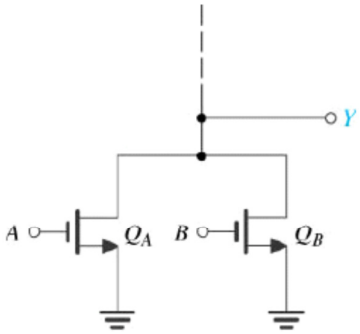




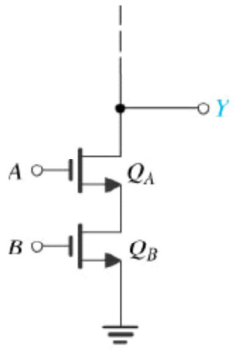
Assumendo approx. forma triangolare per impulso di corrente:

$$P_{SS} = V_{DD} I_{max} \frac{1}{2} (t_{rise} + t_{fall}) f$$

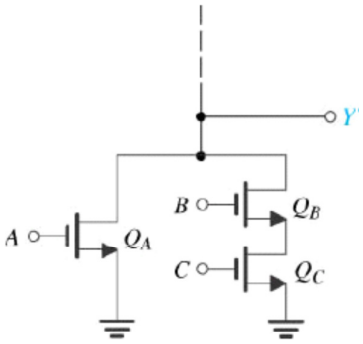
Esempi di reti logiche CMOS:



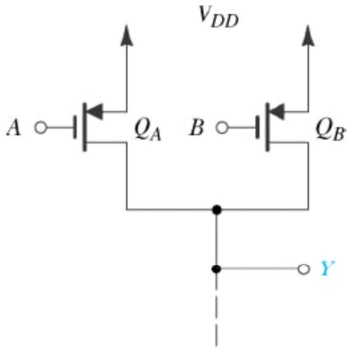
$\overline{Y} = A + B$



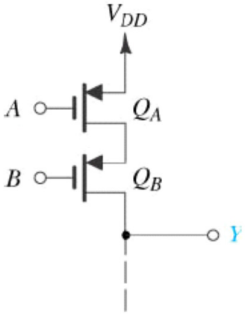
$\overline{Y} = A\,B$



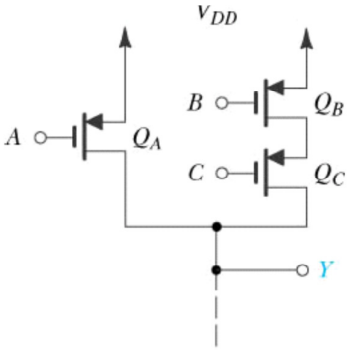
$\overline{Y} = A + BC$



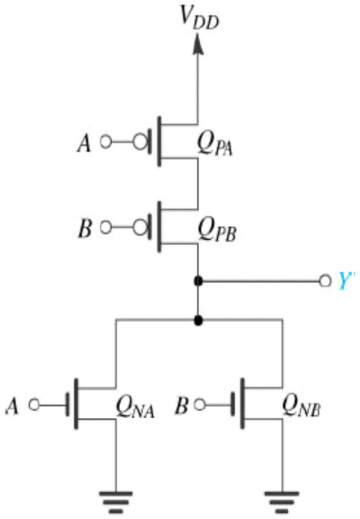
$Y = \overline{A} + \overline{B}$



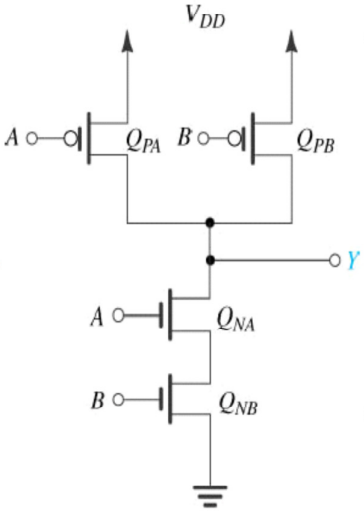
$Y = \overline{A}\,\overline{B}$



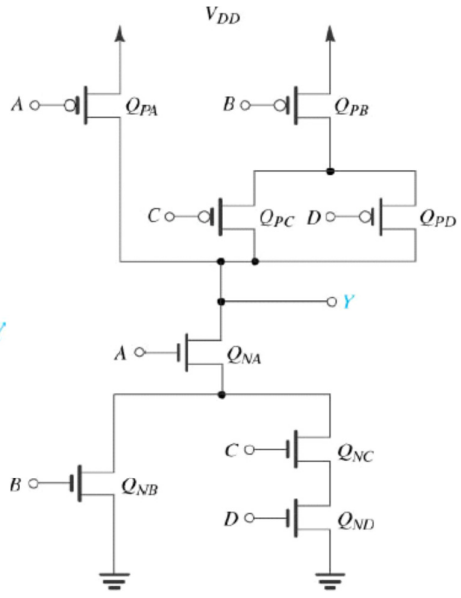
$Y = \overline{A} + \overline{B}\,\overline{C}$



$Y = \overline{A + B}$



$Y = \overline{AB}$



$Y = \overline{A(B + CD)}$