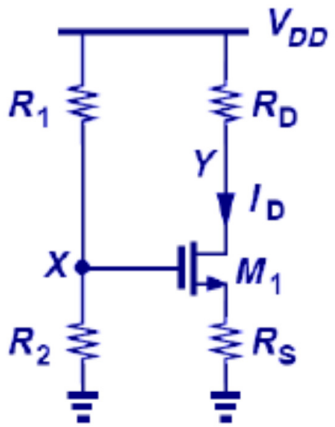
Polarizzazione (= bias) del MOS:
Come per BJT, JFET $\rightarrow$ Necessaria a fissare il punto di lavoro

I_D, V_{GS}, V_{DS} quiescenti:
Valori intorno ai quali
correnti e tensioni di segnale incrementano/decrementano

1) Schema semplice



$\frac{R_2}{R_1+R_2}V_{DD} = V_{GS} + I_D R_S$ maglia di ingresso

$I_D \approx \frac{1}{2}\mu_n C_{0x}\frac{W}{L}\left(V_{GS}-V_{TH}\right)^2$ NMOS

$\rightarrow$ 2 eq. , 2 incognite $\rightarrow V_{GS}, I_D$

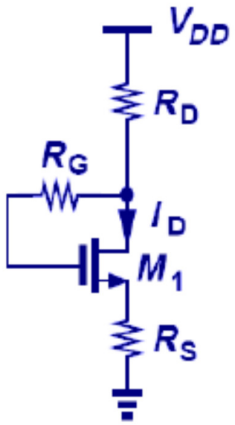
$$V_{GS} = -\left(V_1 - V_{TH}\right) + \sqrt{V_1^2 + 2V_1\frac{R_2}{R_1+R_2}\left(V_{DD}-V_{TH}\right)}$$

$$V_1 = \frac{1}{\mu_n C_{0x}\frac{W}{L}R_S}$$

NB:

Unita' di V_1 : $\frac{1}{\frac{\frac{cm}{s}}{\frac{V}{cm}}Fcm^{-2}\Omega} \rightarrow \frac{1}{\frac{cm}{s}\frac{cm}{V}Fcm^{-2}\Omega} \rightarrow \frac{Vs}{\underbrace{F\Omega}_{s}} \rightarrow V$!!!

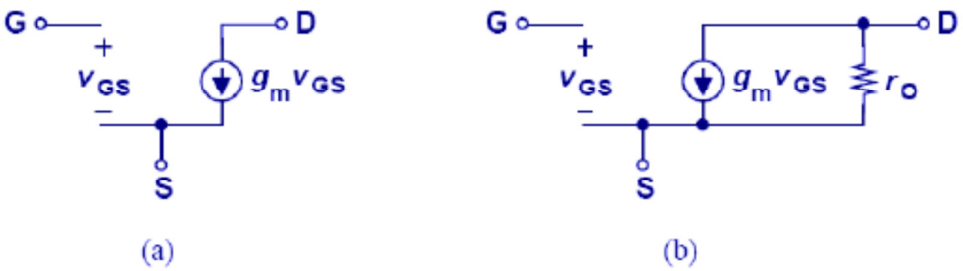
2) Schema a self-bias



$$I_D R_D + V_{GS} + R_S I_D = V_{DD}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2$$

Modello del MOS per piccoli segnali:



$$I_D = \frac{1}{2}\mu_n C_{0x}\frac{W}{L}(V_{GS}-V_{TH})^2\left[1+\underbrace{\lambda(V_{DS}-V_{DS,sat})}_{\substack{\text{correzione}\\ \text{gen. corr. non ideale}\\ \lambda \text{ piccolo}}}\right]$$

$$\rightarrow i_D = \frac{\partial I_D}{\partial V_{GS}}v_{GS}+\frac{\partial I_D}{\partial V_{DS}}v_{DS}+\underbrace{\cancel{\frac{\partial I_D}{\partial V_{BS}}v_{BS}}}_{\substack{\text{Dipendenza}\\ \text{da tensione}\\ \text{source-substrato}\\ \text{trascurata}}}$$

Transconduttanza del NMOS:

$$\frac{\partial I_D}{\partial V_{GS}} \equiv g_m \simeq \mu_n C_{0x}\frac{W}{L}(V_{GS}-V_{TH}) \approx \sqrt{2\mu_n C_{0x}\frac{W}{L}I_D} \approx \frac{2I_D}{V_{GS}-V_{TH}}$$

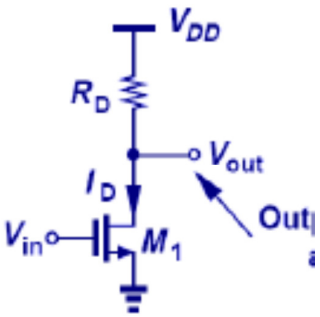
Conduttanza di uscita del NMOS:

$$\frac{\partial I_D}{\partial V_{DS}} \equiv g_0 \equiv \frac{1}{r_0} = \frac{1}{2}\mu_n C_{0x}\frac{W}{L}(V_{GS}-V_{TH})^2\lambda \approx I_D\lambda$$

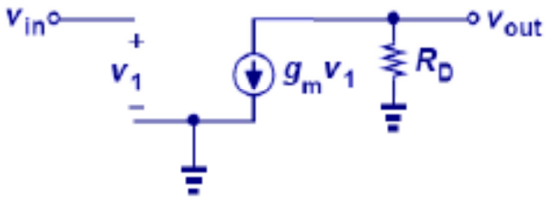
$$\rightarrow r_0 \approx \frac{1}{\lambda I_D}$$

Simile per PMOS

Applicazione: Amplificatore Common Source (CS)



Modello per piccoli segnali:



Guadagno di tensione:

$$\lambda = 0$$
$$A_v = -g_m R_D$$
$$A_v = -\sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} R_D$$

Condizione di saturazione (richiesta per amp. lineare):

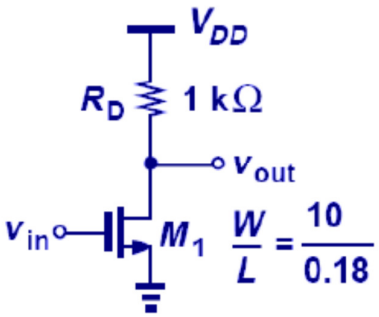
$$V_{out} > V_{in} - V_{TH}$$
$$\rightarrow V_{DD} - I_D R_D > V_{GS} - V_{TH}$$

Es:

$$\left.\begin{array}{l} V_{DD} = +10V \\ V_{TH} = 1.5V \\ I_D = 5\ mA \end{array}\right\} \rightarrow 10 - 10^3 I_D > V_{in} - 1.5$$

$$\rightarrow V_{in} < 10 + 1.5 - 10^3 I_D = 11.5 - 10^3 I_D$$

$$\rightarrow V_{in} < 11.5 - 5\ V = 6.5\ V$$



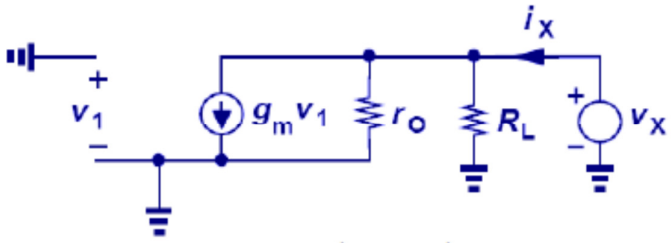
Parametri del 4-polo equivalente:

$A_v = -g_m R_L$

$R_{in} = \infty$

$R_{out} = R_D$

Tenendo conto della variazione della lunghezza del canale con V_{DS}: $r_0 < \infty$



$A_v = -g_m \left(R_D \parallel r_0 \right) \rightarrow A_v \propto R_D$

$R_{in} = \infty$

$R_{out} = R_D \parallel r_0$

Osservazioni generali:

$g_m \left(MOS \right) \ll g_m \left(BJT \right) \rightarrow A_v$ grande richiede R_D grande

R grandi non benvenute in circuiti VLSI

Grandi → occupazione suolo pubblico

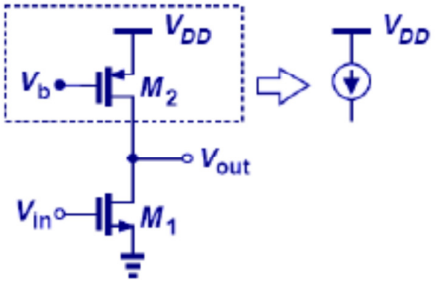
Dissipatrici → riscaldamento globale

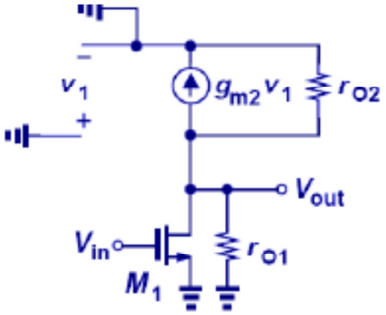
Grande 'Voltage Headroom' → V_{DD} elevata

→ Schemi con generatore di corrente ≡ carico attivo

Resistenza (ohmica) sul drain di M_1 R_D → Res. (dinamica) di uscita di M_2 r_{02}

Non necessaria R_D elevata → Non necessaria V_{DD} elevata



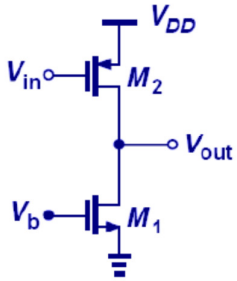


$$A_v = -g_{m1}\left(r_{01} \parallel r_{02}\right)$$

Considerevole simmetria rispetto a scambio NMOS ↔ PMOS:

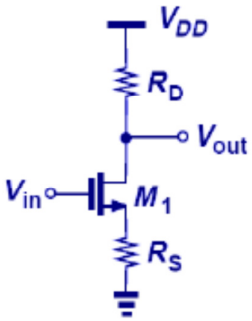
Stesso guadagno

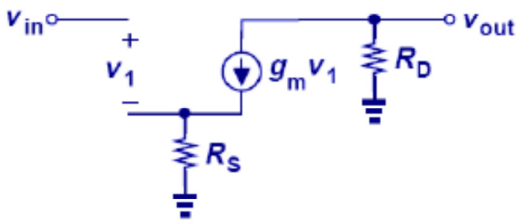
$$A_v = -g_{m2}\left(r_{02} \parallel r_{01}\right)$$



$$A_v = -g_{m2}(r_{O1} \parallel r_{O2})$$

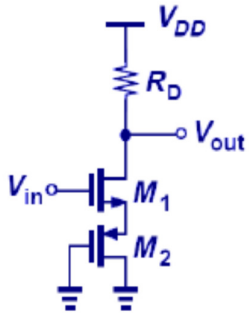
CS con resistenza sul source $\left(\text{assumendo } r_0\right)$:

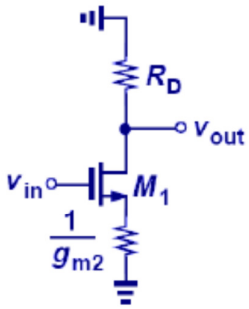




$$A_v = -\frac{R_D}{\frac{1}{g_m} + R_S}$$

PMOS in saturazione invece di una resistenza:

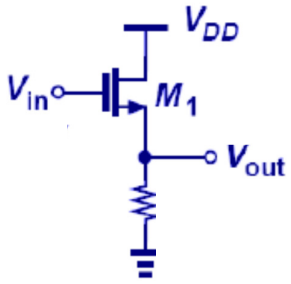


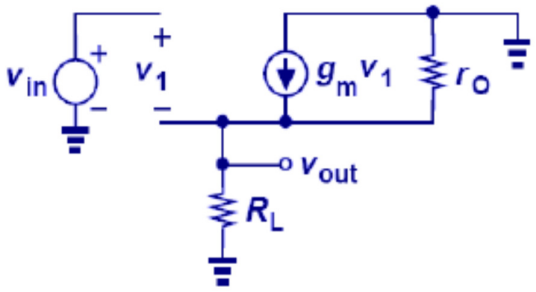


$$A_v = -\frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

Altre configurazioni: Simili a quelle di BJT, JFET

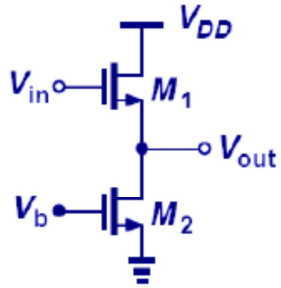
Es.: Source follower

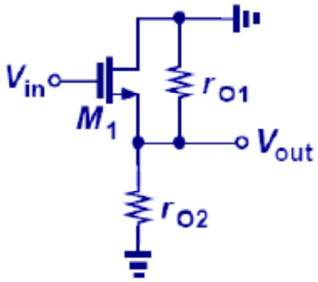




$$\frac{v_{out}}{v_{in}} = \frac{r_O \parallel R_L}{\frac{1}{g_m} + r_O \parallel R_L}$$

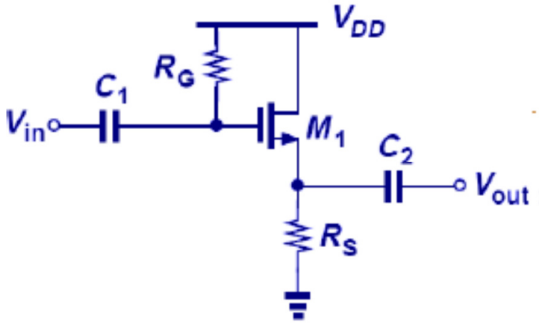
Con carico attivo:





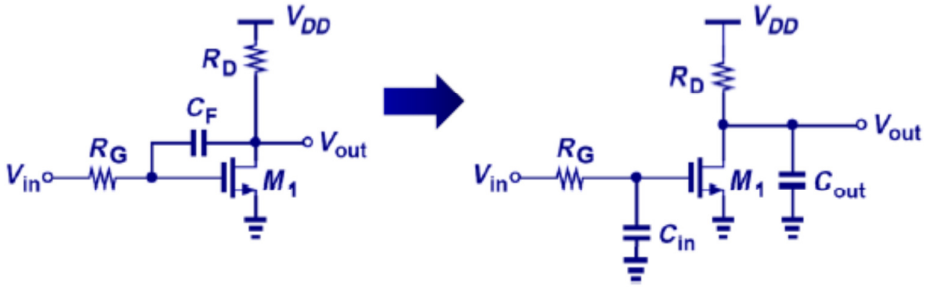
$$A_v = \frac{r_{O1} \parallel r_{O2}}{\frac{1}{g_{m1}} + r_{O1} \parallel r_{O2}}$$

Con polarizzazione:



Comportamento del MOS ad alta frequenza:
Effetto delle capacita' intrinseche

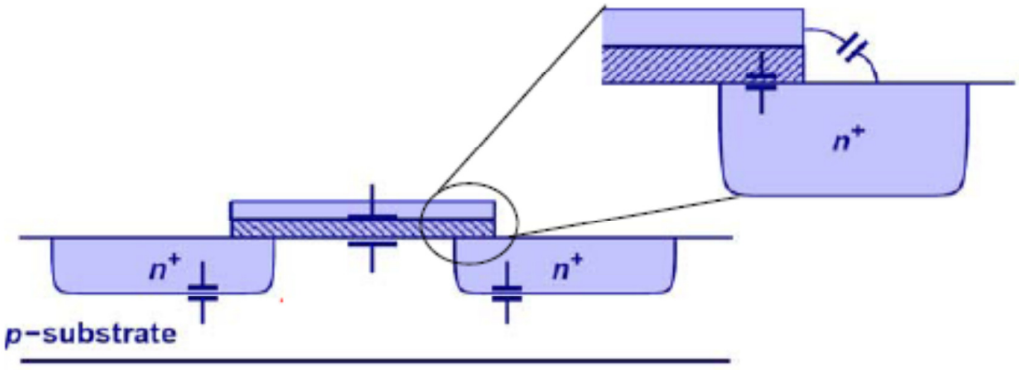
Problema simile a quello del BJT: Effetto Miller
→ Teorema di Miller per decomposizione C_F



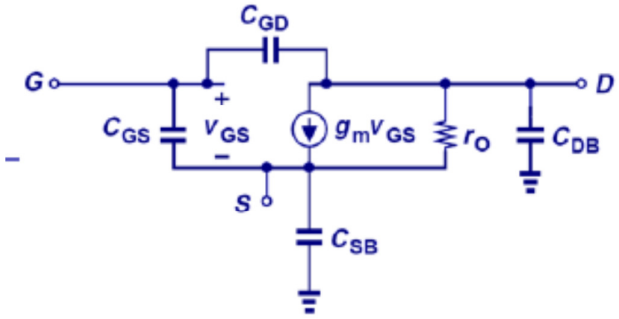
$$\omega_{in} = \frac{1}{R_G(1+g_m R_D)C_F} \qquad \omega_{out} = \frac{1}{R_D\left(1+\frac{1}{g_m R_D}\right)C_F}$$

Capacita' intrinseche del MOS:

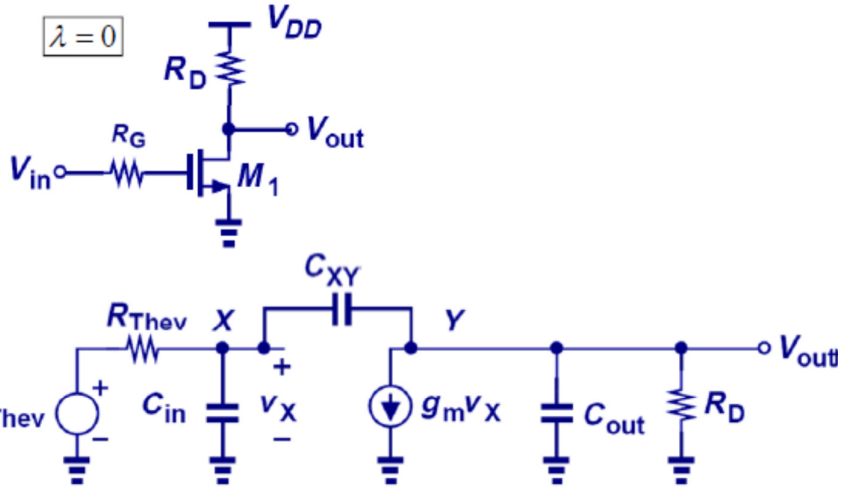
Gate-Canale
Gate-Source e Gate-Drain (Cap. di overlap e da fringing field)
Source-Body e Drain-Body (Cap. di giunzione)



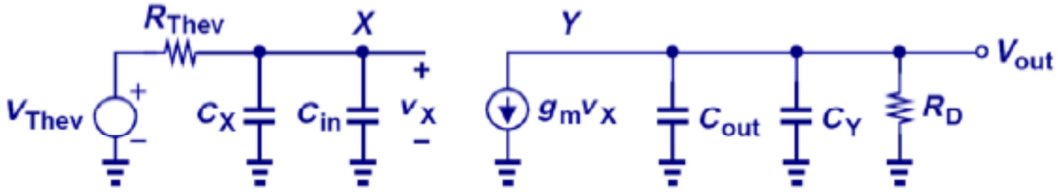
Modello del MOS con capacita':



Applicazione: Stadio a source comune (CS)



Con teorema di Miller:



$$V_{Thev} = V_{in}$$

$$R_{Thev} = R_G$$

$$C_X = C_{GD}\,(1 + g_m R_D)$$

$$C_Y = C_{GD}\left(1 + \frac{1}{g_m R_D}\right)$$

$$\omega_{p,in} = \frac{1}{R_{Thev}\left(C_{in} + \left(1 + g_m R_D\right) C_{GD}\right)}$$

$$\omega_{p,out} = \frac{1}{R_D\left(C_{out} + \left(1 + \frac{1}{g_m R_D}\right) C_{GD}\right)}$$

Applicazione: Stadio CS con carico attivo

Stadio CS carico attivo PMOS

Capacita' intrinseche

Semplificato