Famiglie logiche:

Inizio '900: Rele'
(es. centralini telefonici, Z3 (Germania - 1941))

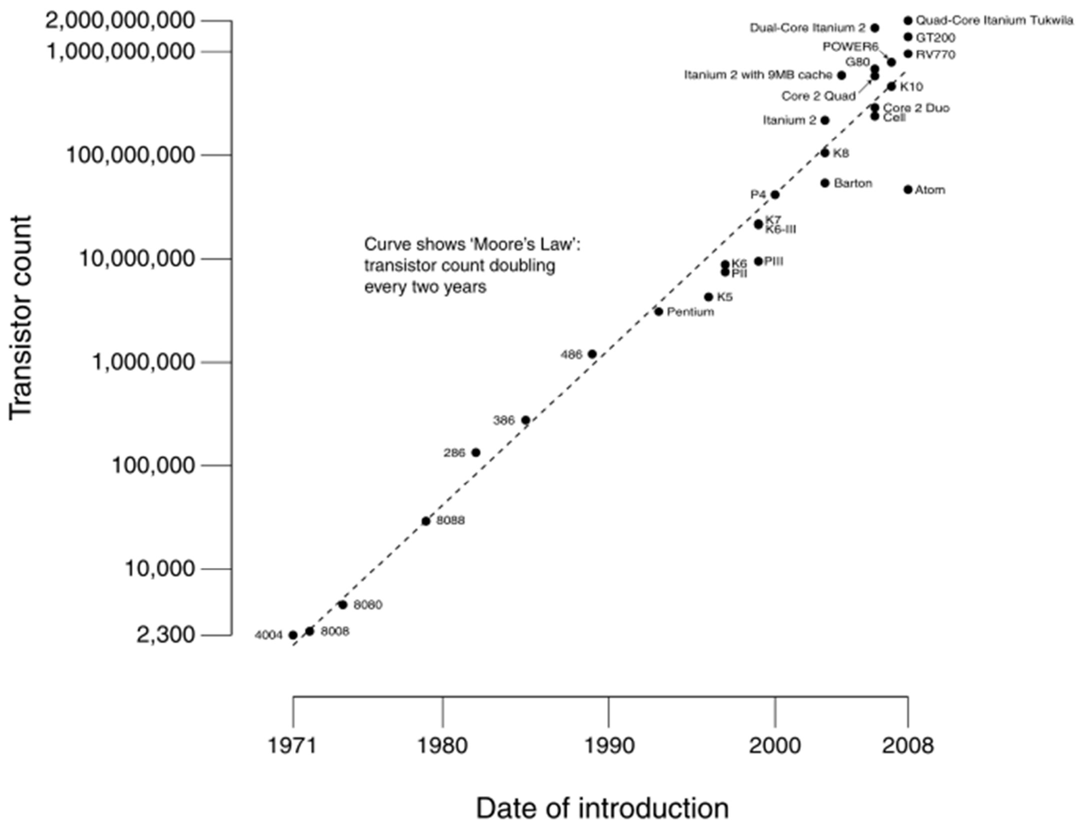
Anni '40-'50: Tubi a vuoto
(es. ENIAC (US - 1946))

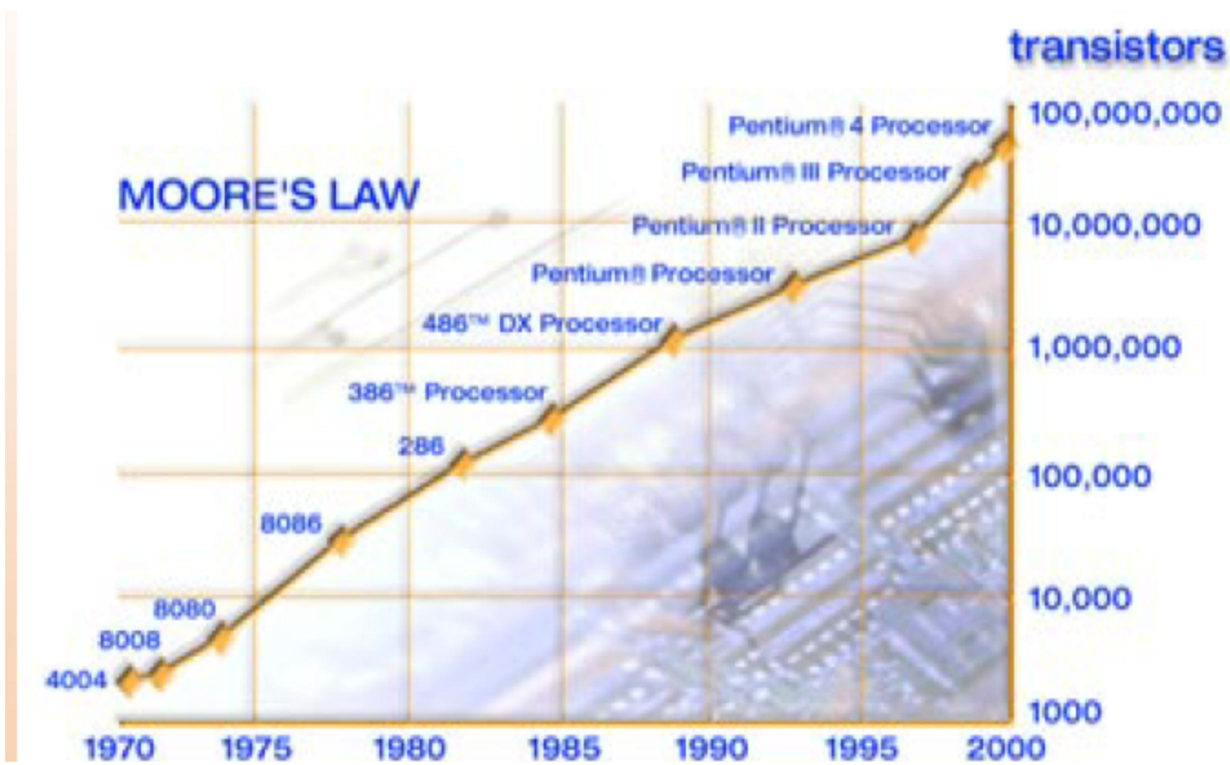
Anni '60: Transistor bipolari
(Discreti, poi integrati - Es. RTL, DTL, TTL,...)

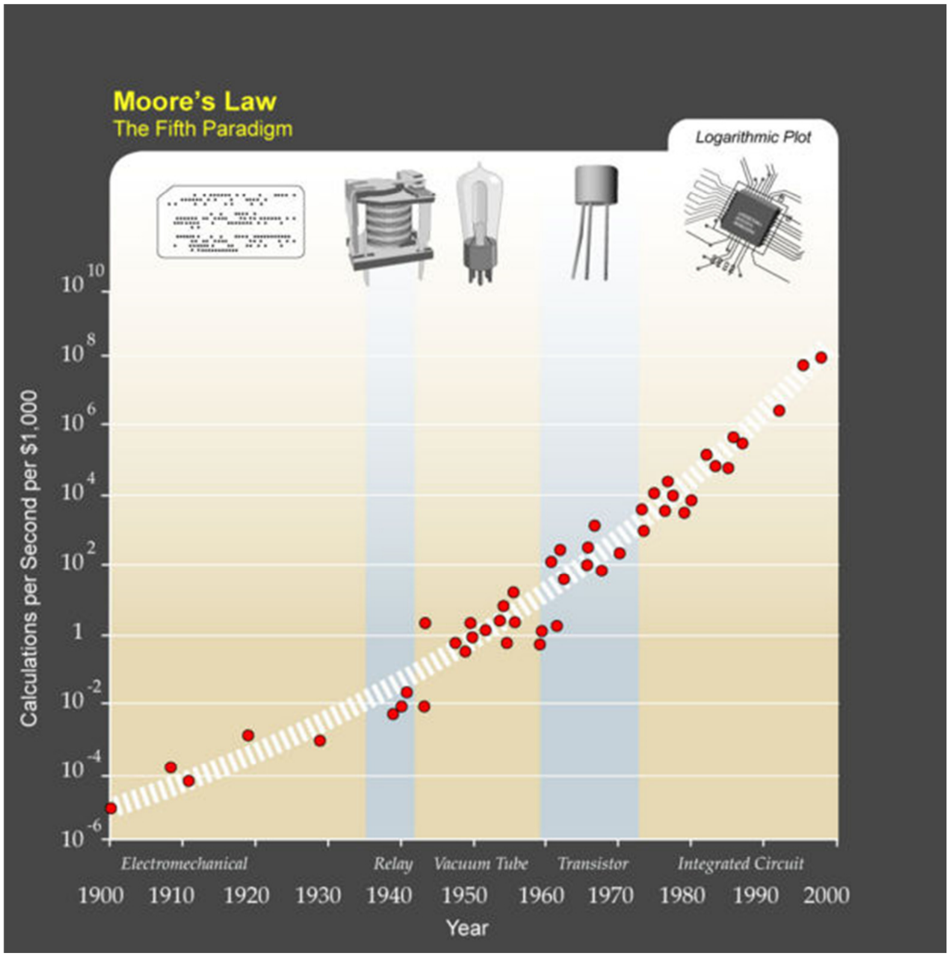
Anni '70 - '80: PMOS, NMOS
(Zilog Z80, Intel 8080, Motorola 6502, Fairchild F8, ..)

Anni '90 $\rightarrow$: CMOS
$\sim$ Tutto!

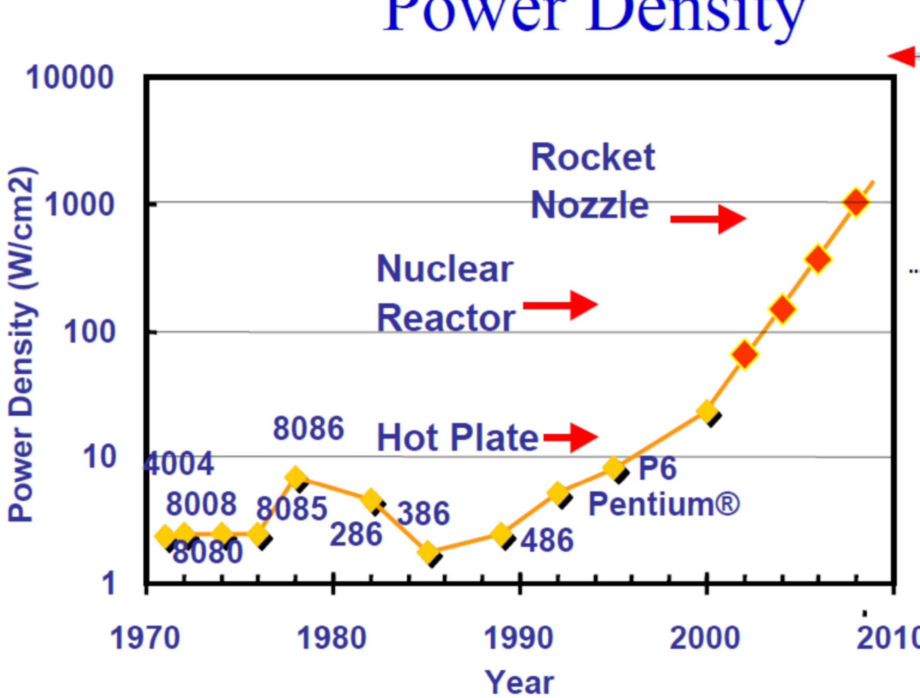
CPU Transistor Counts 1971-2008 & Moore's Law



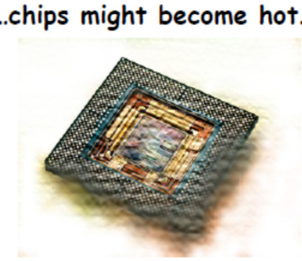




Power Density

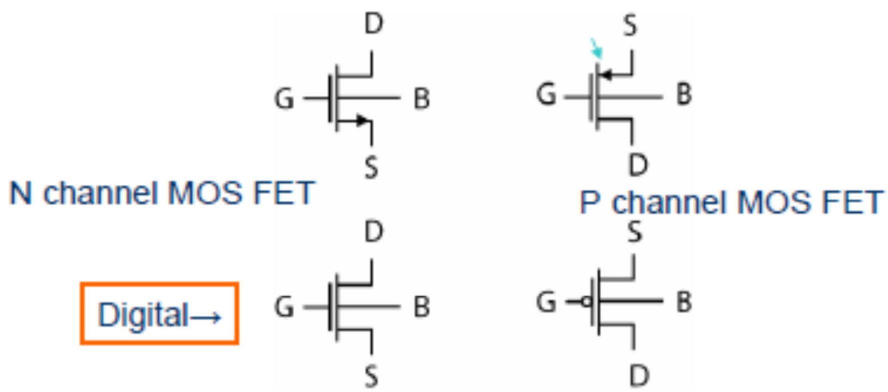


...chips might become hot...

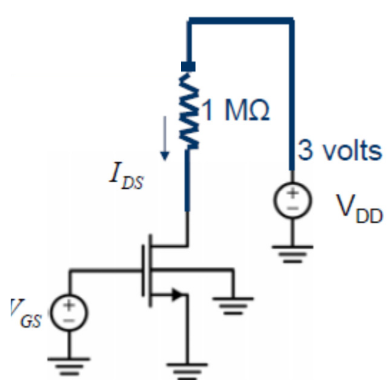


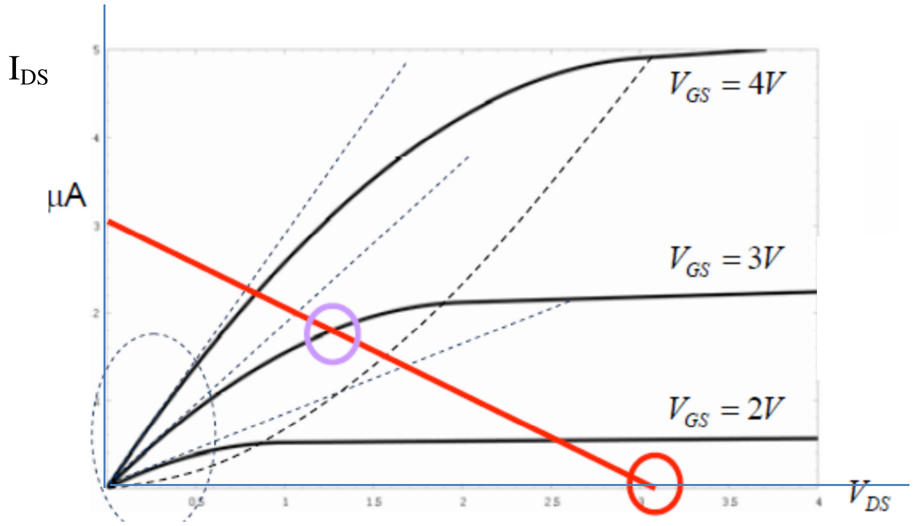
MOS usati come interruttori:

NMOS ON per VG +va
PMOS ON per VG -va



Inverter NMOS:





Input HIGH Input LOW

$\rightarrow$ Per input $HIGH$, output $\sim 1.2V$

$\rightarrow$ Stadio successivo pilotato da un LOW troppo alto

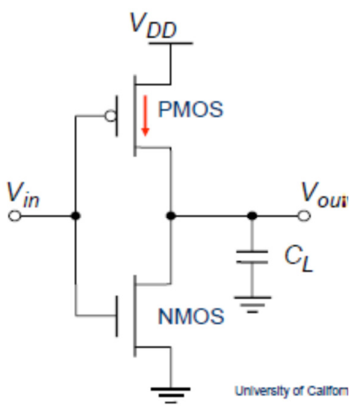
Inoltre:

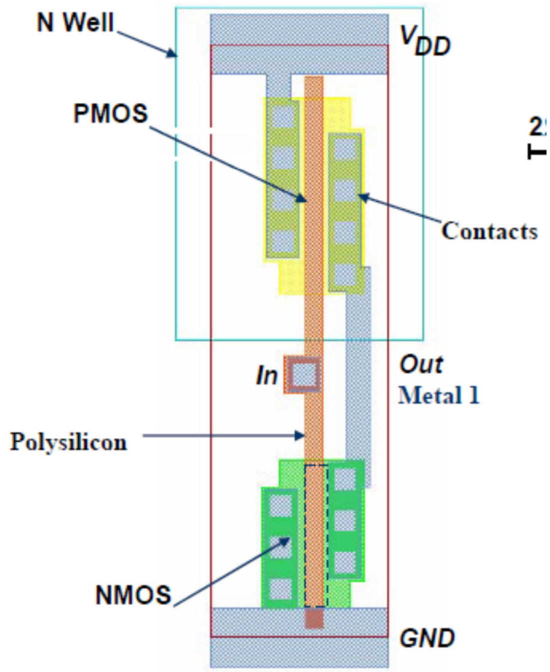
R grandi difficili e non benvenute

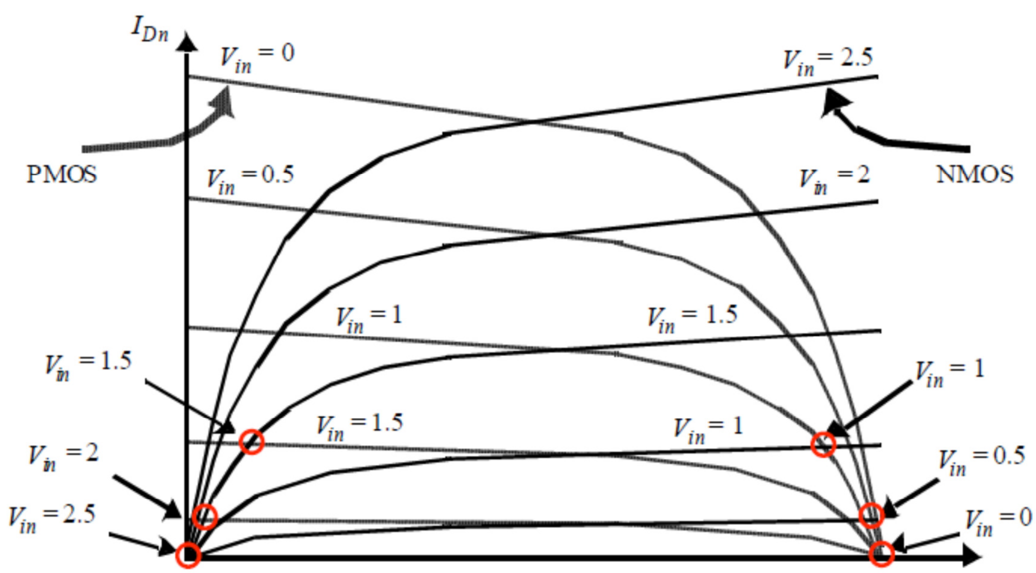
$I_{LOW} \sim 3\mu A \rightarrow P_{inv} \sim 10\mu W \rightarrow P_{tot} \sim 1\ W\,/\,10^5\, transistor$

$(1\ CPU$ di oggi $\sim 10kW\ !)$

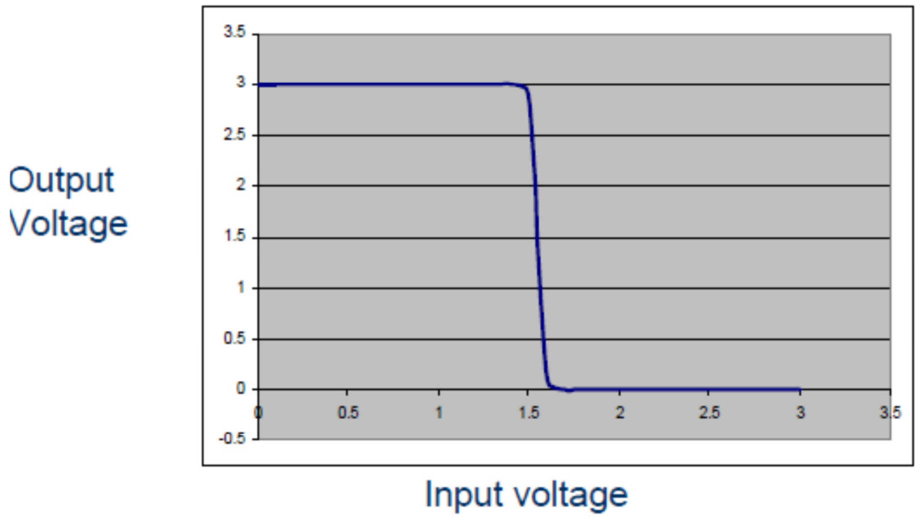
Inverter CMOS:



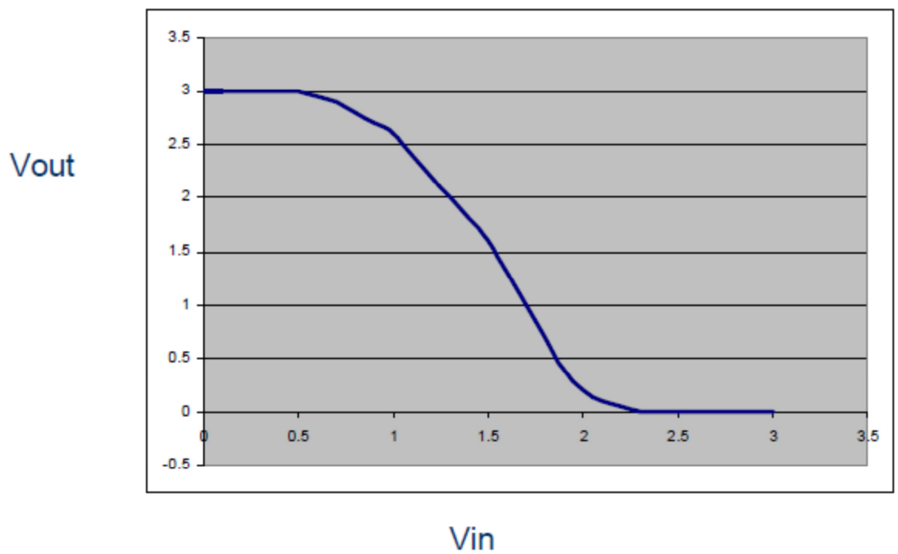


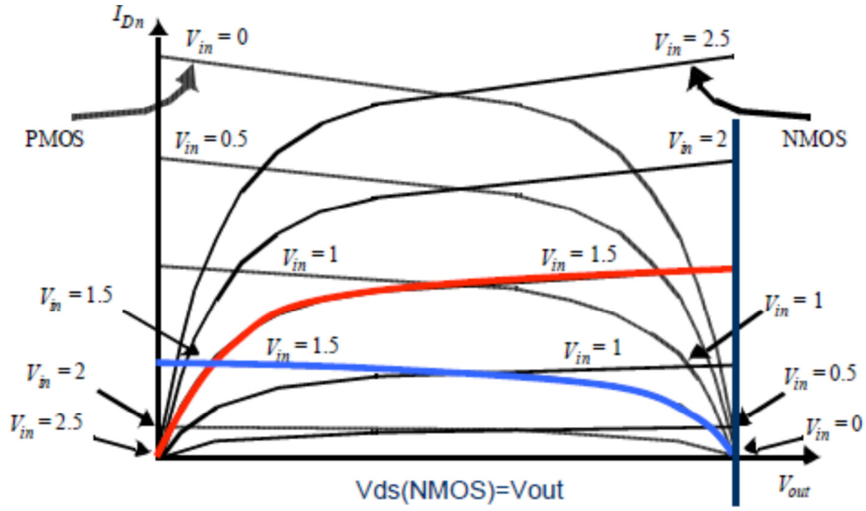


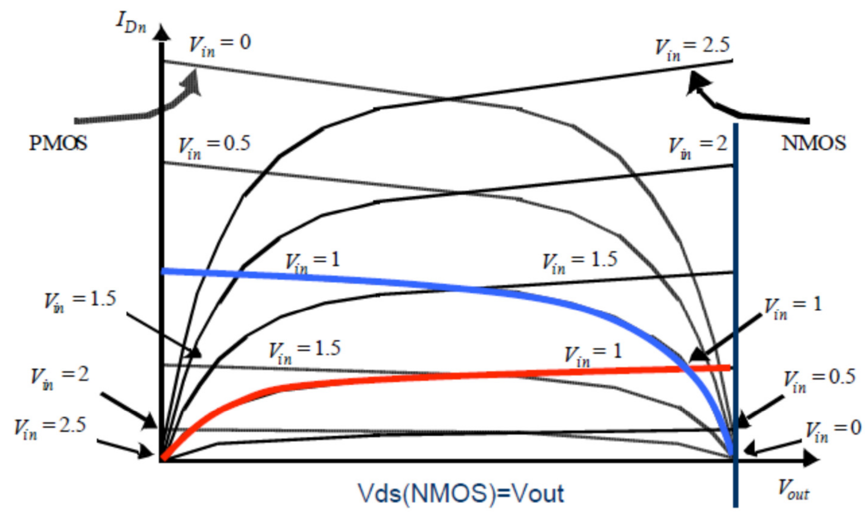
Risposta in/out di un inverter 'ideale':

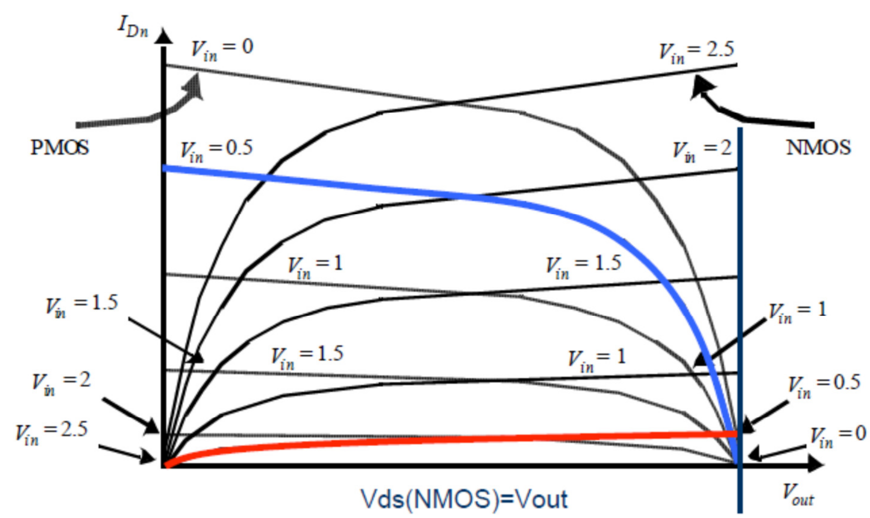


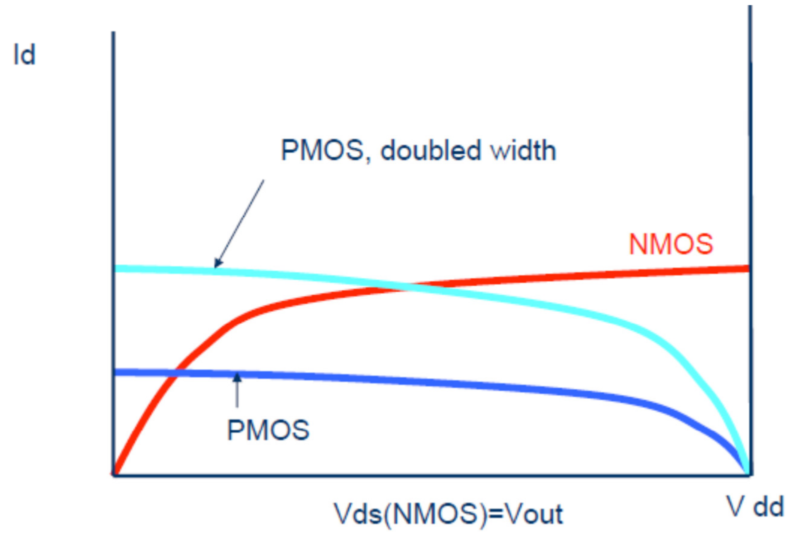
Risposta in/out di un inverter CMOS:




I_{Dn}
$V_{in} = 0$
$V_{in} = 2.5$
PMOS
NMOS
$V_{in} = 0.5$
$V_{in} = 2$
$V_{in} = 1$
$V_{in} = 1.5$
$V_{in} = 1.5$
$V_{in} = 1$
$V_{in} = 1.5$
$V_{in} = 1$
$V_{in} = 2$
$V_{in} = 0.5$
$V_{in} = 2.5$
$V_{in} = 0$
Vds(NMOS)=Vout
V_{out}


I_{Dn}
$V_{in} = 0$
$V_{in} = 2.5$
PMOS
NMOS
$V_{in} = 0.5$
$V_{in} = 2$
$V_{in} = 1$
$V_{in} = 1.5$
$V_{in} = 1.5$
$V_{in} = 1$
$V_{in} = 1.5$
$V_{in} = 1$
$V_{in} = 2$
$V_{in} = 0.5$
$V_{in} = 2.5$
$V_{in} = 0$
Vds(NMOS)=Vout
V_{out}


I_{Dn}
$V_{in} = 0$
$V_{in} = 2.5$
PMOS
NMOS
$V_{in} = 0.5$
$V_{in} = 2$
$V_{in} = 1$
$V_{in} = 1.5$
$V_{in} = 1.5$
$V_{in} = 1$
$V_{in} = 1.5$
$V_{in} = 1$
$V_{in} = 2$
$V_{in} = 0.5$
$V_{in} = 2.5$
$V_{in} = 0$
Vds(NMOS)=Vout
V_{out}



V_M tensione di drain comune

Corrente per NMOS

$$I_{Dn} = v_{sat,n} W_n C_{0x} \left(V_M - V_{Tn}\right)^2 \left(1 + \lambda_n V_M\right)$$

Corrente per PMOS

$$I_{Dp} = -I_{Dn} = v_{sat,p} W_n C_{0x} \left(V_{DD} - V_M + V_{Tp}\right)^2 \left(1 + \lambda_p \left(V_{DD} - V_M\right)\right)$$

$$g_n = v_{sat,n} W_n C_{0x}$$

$$g_p = v_{sat,p} W_p C_{0x}$$

Trascurando i λ:

$$v_{sat,p} W_p C_{0x} \left(V_{DD} - V_M + V_{Tp}\right)^2 \approx v_{sat,n} W_n C_{0x} \left(V_M - V_{Tn}\right)^2$$

$$\rightarrow g_p \left(V_{DD} - V_M + V_{Tp}\right)^2 \approx g_n \left(V_M - V_{Tn}\right)^2$$

$$\rightarrow V_{DD} - V_M + V_{Tp} \approx \sqrt{\frac{g_n}{g_p}} \left(V_M - V_{Tn}\right)$$

$$\rightarrow V_M \left(1 + \sqrt{\frac{g_n}{g_p}}\right) \approx \sqrt{\frac{g_n}{g_p}} V_{Tn} + V_{Tp} + V_{DD}$$

$$\rightarrow V_M \approx \frac{\sqrt{\frac{g_p}{g_n}} \left(V_{DD} + V_{Tp}\right) + V_{Tn}}{1 + \sqrt{\frac{g_p}{g_n}}}$$

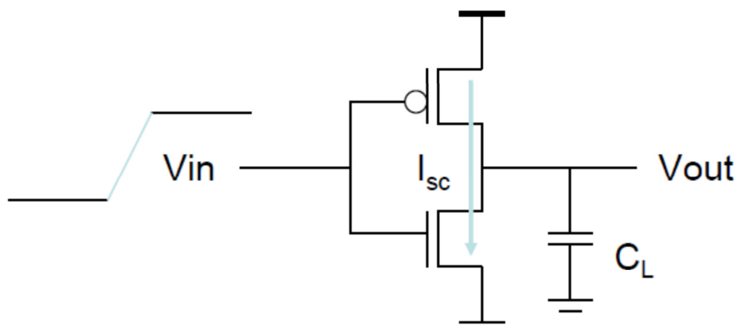
Nessuna potenza dissipata staticamente

Ma: potenza dissipata *dinamicamente*

$\rightarrow$ Durante le transizioni

$\rightarrow$ Carica e scarica del carico capacitivo

$\left(\leftarrow C_{out}\left(\text{stadio } n\right)+C_{in}\left(\text{stadio } n+1\right)\right)$



$i_L = C_L \dfrac{dv_O}{dt}$ corrente nella capacita'

$P_P = i_L V_{DS} = i_L\left(V_{DD} - V_O\right)$ Pot. istantanea dissipata dal PMOS

$E_P = \int_0^\infty P_P\left(t\right)dt = \int_0^\infty C_L\left(V_{DD} - V_O\right)\dfrac{dv_O}{dt}dt$ Energia

$\rightarrow E_P = \int_0^{V_{DD}} C_L\left(V_{DD} - V_O\right)dv_O = C_L V_{DD}^2 - \dfrac{1}{2}C_L V_{DD}^2 = \dfrac{1}{2}C_L V_{DD}^2$

$\rightarrow E_N = \dfrac{1}{2}C_L V_{DD}^2$ En. dissipata nel NMOS

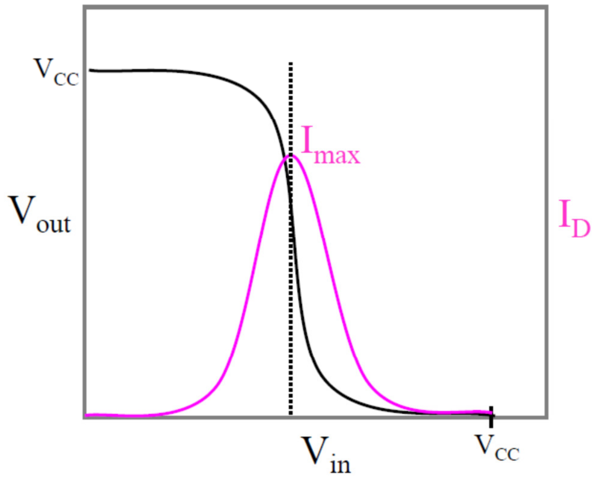
$\rightarrow E_T = C_L V_{DD}^2$ En. totale dissipata

Pot. dissipata:

$P = fE_T = fC_L V_{DD}^2$

Inoltre:

Passaggio di corrente nell'inverter durante le transizioni



Pot. dissipata

$$P_{SC} \simeq V_{DD} I_{\max} \frac{t_{sal} + t_{disc}}{2} f$$

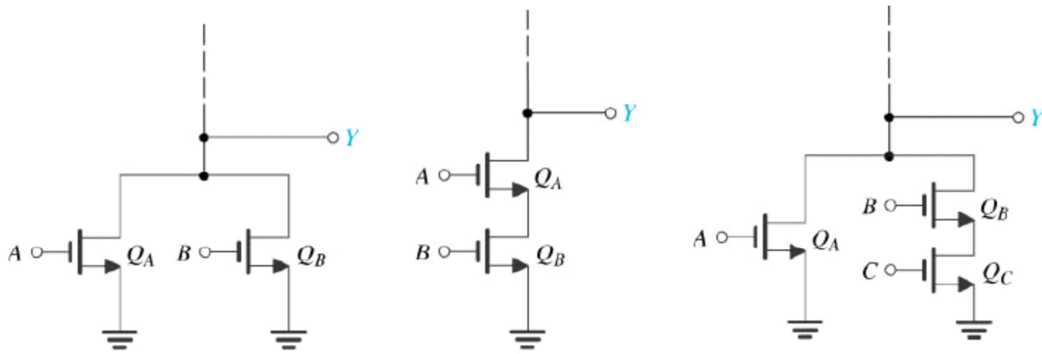
Inoltre:

Piccola potenza dissipata staticamente (correnti residue)

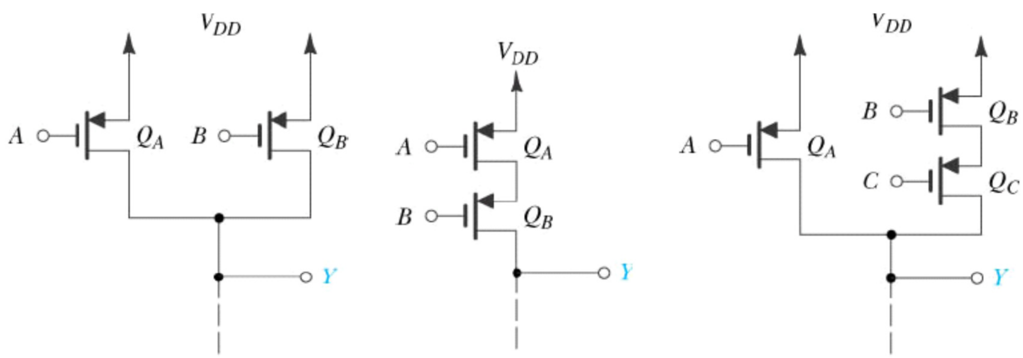
Totale:

$$P_{tot} = f C_L V_{DD}^2 + V_{DD} I_{\max} \frac{t_{sal} + t_{disc}}{2} f + P_{stat}$$

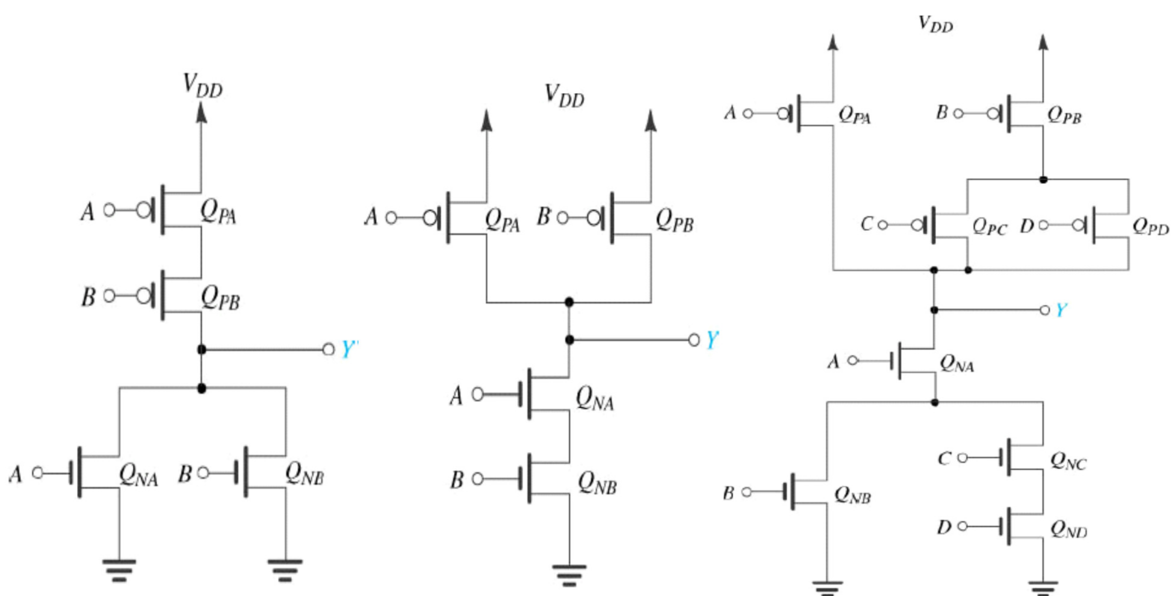
Esempi di reti logiche CMOS:



$\overline{Y} = A + B$ $\overline{Y} = A\,B$ $\overline{Y} = A + BC$



$Y = \overline{A} + \overline{B}$ $Y = \overline{A}\,\overline{B}$ $Y = \overline{A} + \overline{B}\,\overline{C}$



$Y = \overline{A + B}$ $Y = \overline{AB}$ $Y = \overline{A(B + CD)}$